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BROWDY AND NEIMARK, P.L.L.C.
624 NINTH STREET, NW
SUITE 300
WASHINGTON, DC 20001-5303

EXAMINER	
TRUONG, CAM Y T	
ART UNIT	PAPER NUMBER
2162	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,393	RINDNER, YOSSI	
	Examiner	Art Unit	
	Cam Y T. Truong	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-13 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant has amended claims 5, 12 and added claim 16 and withdrawn claims 14-15 in the amendment file on 5/26/2005. Claims 5-13 and 16 are pending in this Office Action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued on pages 7-10 that there is no motivation to combine the teachings of Duboc and Gupte; nothing about the selectors being part of the templates".

Examiner respectfully disagrees the entire allegation as argued. Examiner, in her previous office action, gave detail explanation of claimed limitation and pointed out exact locations in the cited prior art.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of HDL code defining the ASIC is checked against

rules, and guidelines that ensure correct-by construction designs to Duboc's system in order to simulate and verify the correctness of an HDL hardware model easily and further to allow an integrated circuit to be modeled at a variety of an abstraction levels.

"Test of obviousness is not whether features of secondary reference may be bodily incorporated into primary reference's structure, nor whether claimed invention is expressly suggested in any one or all of references; rather, test is what combined teachings of references would have suggested to those of ordinary skill in art."

In re Keller, Terry, and Davies, 208 USPQ 871 (CCPA 1981).

"Reason, suggestion, or motivation to combine two or more prior art references in single invention may come from references themselves, from knowledge of those skilled in art that certain references or disclosures in references are known to be of interest in particular field, or from nature of problem to be solved;" Pro-Mold and Tool Co. v. Great Lakes Plastics Inc. U.S. Court of Appeals Federal Circuit 37 USPQ2d 1626 Decided February 7, 1996 Nos. 95-1171, -1181

"[q]uestion is whether there is something in prior art as whole to suggest desirability, and thus obviousness, of making combination." Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Company et al. U.S. Court of Appeals Federal Circuit 221 USPQ 481 Decided Mar. 21, 1984 No 83-1178.

In response to applicant argument, nothing about the selectors being part of the templates, Duboc teaches the selected selector such as button 224 is part of template as DSP builder template (fig. 6).

In view of the above, the examiner contends that all limitations as recited in the claims have been addressed in this Action.

For the above reason, examiner believed that rejection of the last office action was proper.

Claim Objections

3. Claim 9 is objected to because of the following informalities:

Claim 9 recites the claimed limitation "wherein the pre-prepared template is part of the selected selectors" on page 4, lines 6-7. The language for this claimed limitation is incorrect according to the description of the application, a template includes a plurality of selectors i.e. button (fig. 1, page 7, lines 15-18). Thus, base on the description of the application, examiner interprets this claimed limitation as the selected selectors are parts on the pre-prepared template.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-9, 12, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Gupte et al (or hereinafter "Gupte") (US 5903475).

As to claim 5, Duboc teaches an apparatus for interfacing between first and second successive stages of an ASIC synthesis tool (fig. 5, col. 8, lines 25-36), said apparatus comprising:

"a processor" as processor 31 (fig. 2),

"a plurality of selectors coupled to the processor" as a compile button 224 and a cancel option is provided by a close button 226, optional circuit blocks that can select by a user via a user interface are coupled to the processor 31. The buttons and circuit blocks are represented as selectors (figs. 2&6, col. 10, lines 20-25; col. 5, lines 60-63);

"each corresponding to a tool for performing a stage in an ASIC design" as a compile option or button 224 is corresponding to the HDL Integrator tool. Circuit blocks are corresponding to a design reuse tool or the HDL Integrator tool. The user initiates generation of the integrated circuit design via selection of a compile option or button 224 from the GUI window. In this case, the step user initiates generation of the integrated

circuit design via selection of a compile option from the GUI window is represented as a stage in a circuit design (col. 8, lines 33-38; col. 10, lines 20-25; col. 5, lines 60-63);

"a memory coupled to the processor and storing therein respective script files relating to each of said selectors" as memory 32 is coupled to processor 31. The template may also generate one or more script files, including IIDLI scripts utilized to extract instantiated blocks from the design reuse tool database to extract instantiated blocks from the design reuse tool database. In addition, scripts for running the memory Integrator tool, as well as compilation and simulation script, may be generated to simulate the subsystem. The above information implies that generated script files has stored in the memory for extracting instantiated blocks as selectors (fig. 5, col. 10, lines 58-64);

"said processor being responsive to selection of at least one of the selectors for accessing the memory and executing commands associated therewith" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory and executing a check script 154 and a build script 162. Script 153 and 162 are represented as commands associated with the compile option (figs. 2&5, col. 8, lines 33-49);

"wherein the tool for performing a stage in the ASIC design is one of a DFT (Design For test) unit, a static verification unit, a physical compile unit, a physical STA (Static Timing Analysis) unit and an ECO (Electronic Change Order) unit" as to facilitate the design of integrated circuits, software programs, also referred to as "tools", have been developed to permit a developer to define an integrated circuit design at a

relatively higher conceptual level, and then have operations such as synthesizing the physical layout of the integrated circuit design, testing the integrating circuit design, etc., performed automatically by the tool. Thus, each program is represented as a DFT unit (col. 1, lines 37-45).

Duboc does not explicitly teach the claimed limitation "the tool is not an ASIC synthesis tool". Gupte teaches HDL is a programming language that is used to model digital systems at many levels of abstraction ranging from the algorithmic level to the gate level. HDL has many uses including behavioral specification, gate level specification, and implementation of test benches. The HDL code, which defines the ASIC is checked against rules and guideline that ensure correct-by-construction designs. As shown in fig. 12, the HDL code and design specific synthesis scripts are combined to synthesis tool 714. Thus the HDL code, which is a tool, is not an synthesis tool 714 (fig. 12, col. 1, lines 15-40; col. 6, lines 65-67).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of HDL code defining the ASIC is checked against rules, and guidelines that ensure correct-by construction designs to Duboc's system in order to simulate and verify the correctness of an HDL hardware model and further to allow an integrated circuit to be modeled at a variety of an abstraction levels.

As to claim 6, Duboc teaches the claimed limitation "wherein the commands executed by the processor are extracted from the respective script file relating to each of said selected selectors" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory to retrieve instructions of the check script 154 from a script file related to selected blocks or compile option (figs. 2&5, col. 8, lines 33-49; col. 10, lines 58-60).

As to claim 9, Duboc teaches the claimed limitation "wherein the pre-prepared template is part of the selected selector" as indicated on the above claims objection, this claimed language is considered as the selected selector such as button 224 is part of template as DSP builder template (fig. 6).

As to claim 12, Duboc teaches the claimed limitation "wherein the commands executed by the processor are related to each of said selected selectors" as indicated on the above claims objection, this claimed language is considered as the commands executed by the processor are related the each of said selected selector. Build script 162 and script 154 are related to compile or button 224 and close or button 226 (fig. 6, col. 8, lines 33-50).

As to claim 13, Duboc teaches the claimed limitation "wherein at least some of said selectors are operable via a graphic user interface" as template permits both the

selection of one or more optional circuit blocks and the customization of one or more customizable circuit blocks to be performed via a user interface (col. 5, lines 60-63).

As to claim 7, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated". Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

As to claim 8, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated according to a pre-prepared template". Duboc teaches a template may also generate one or more script files (col. 10, lines 58-60). Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

As to claim 16, Duboc does not explicitly teach the claimed limitation "wherein the processor is adapted to provide automatic integration with version control tools". Gupte teaches synthesis scripts and hierarchical flow/connectivity diagrams are automatically generated at step 212 (col. 7, lines 10-15).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of synthesis scripts and hierarchical flow/connectivity diagrams are automatically generated to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

6. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Gupte and further in view of Hekmatpour (US 2002/0156929).

As to claim 10, Duboc and Gupte disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared template is a pre-prepared external file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Gupte's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of functional components that includes simulator and synthesis and timing analysis component.

As to claim 11, Duboc and Gupte disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared external template file is an XML file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Gupte's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of functional components that includes simulator and synthesis and timing analysis component.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Gupte and further in view of Kuribayashi (US 6374205).

As to claim 16, Duboc does not explicitly teach the claimed limitation "wherein the processor is adapted to provide automatic integration with version control tools". Kuribayashi teaches designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are essential for automatically designing ASICs (application specific integrated circuits) such as memories, in particular, SRAMs. The automatic designing technology is improving to meet requirements for large-scale memories and a short turn around time (col. 1, lines 19-25).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Kuribayashi's teaching of designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are essential for automatically designing ASICs such as memories, in particular, SRAMs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further improve to meet requirements for large-scale memories and a short turn around time

8. Claims 5, 6, 9, 12, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Kuribayashi.

As to claim 5, Duboc teaches an apparatus for interfacing between first and second successive stages of an ASIC synthesis tool (fig. 5, col. 8, lines 25-36), said apparatus comprising:

"a processor" as processor 31 (fig. 2),

"a plurality of selectors coupled to the processor" as a compile button 224 and a cancel option is provided by a close button 226, optional circuit blocks that can select by a user via a user interface are coupled to the processor 31. The buttons and circuit blocks are represented as selectors (figs. 2&6, col. 10, lines 20-25; col. 5, lines 60-63);

"each corresponding to a tool for performing a stage in an ASIC design" as a compile option or button 224 is corresponding to the HDL Integrator tool. Circuit blocks are corresponding to a design reuse tool or the HDL Integrator tool. The user initiates generation of the integrated circuit design via selection of a compile option or button 224 from the GUI window. In this case, the step user initiates generation of the integrated circuit design via selection of a compile option from the GUI window is represented as a stage in a circuit design (col. 8, lines 33-38; col. 10, lines 20-25; col. 5, lines 60-63);

"a memory coupled to the processor and storing therein respective script files relating to each of said selectors" as memory 32 is coupled to processor 31. The template may also generate one or more script files, including IIDLI scripts utilized to extract instantiated blocks from the design reuse tool database to extract instantiated blocks from the design reuse tool database. In addition, scripts for running the memory Integrator tool, as well as compilation and simulation script, may be generated to simulate the subsystem. The above information implies that generated script files has

stored in the memory for extracting instantiated blocks as selectors (fig. 5, col. 10, lines 58-64);

"said processor being responsive to selection of at least one of the selectors for accessing the memory and executing commands associated therewith" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory and executing a check script 154 and a build script 162. Script 153 and 162 are represented as commands associated with the compile option (figs. 2&5, col. 8, lines 33-49);

"wherein the tool for performing a stage in the ASIC design is one of a DFT (Design For test) unit, a static verification unit, a physical compile unit, a physical STA (Static Timing Analysis) unit and an ECO (Electronic Change Order) unit" as to facilitate the design of integrated circuits, software programs, also referred to as "tools", have been developed to permit a developer to define an integrated circuit design at a relatively higher conceptual level, and then have operations such as synthesizing the physical layout of the integrated circuit design, testing the integrating circuit design, etc., performed automatically by the tool. Thus, each program is represented as a DFT unit (col. 1, lines 37-45).

Duboc does not explicitly teach the claimed limitation "the tool is not an ASIC synthesis tool". Kuribayashi teaches designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are essential for automatically designing ASICs such as memories, in particular, SRAMs. The automatic

designing technology is improving to meet requirements for large-scale memories and a short turn around time (col. 1, lines 19-25).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Kuribayashi's teaching of designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are essential for automatically designing ASICs such as memories, in particular, SRAMs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further improve to meet requirements for large-scale memories and a short turn around time

As to claim 6, Duboc teaches the claimed limitation "wherein the commands executed by the processor are extracted from the respective script file relating to each of said selected selectors" as processor 31 being responsive to selection of a compile option from the GUI window for accessing the memory to retrieve instructions of the check script 154 from a script file related to selected blocks or compile option (figs. 2&5, col. 8, lines 33-49; col. 10, lines 58-60).

As to claim 9, Duboc teaches the claimed limitation "wherein the pre-prepared template is part of the selected selector" as indicated on the above claims objection, this claimed language is considered as the selected selector such as button 224 is part of template as DSP builder template (fig. 6).

As to claim 12, Duboc teaches the claimed limitation "wherein the commands executed by the processor are related to each of said selected selectors" as indicated on the above claims objection, this claimed language is considered as the commands executed by the processor are related the each of said selected selector. Build script 162 and script 154 are related to compile or button 224 and close or button 226 (fig. 6, col. 8, lines 33-50).

As to claim 13, Duboc teaches the claimed limitation "wherein at least some of said selectors are operable via a graphic user interface" as template permits both the selection of one or more optional circuit blocks and the customization of one or more customizable circuit blocks to be performed via a user interface (col. 5, lines 60-63).

As to claim 16, Duboc does not explicitly teach the claimed limitation "wherein the processor is adapted to provide automatic integration with version control tools". Kuribayashi teaches designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are essential for automatically designing ASICs such as memories, in particular, SRAMs. The automatic designing technology is improving to meet requirements for large-scale memories and a short turn around time (col. 1, lines 19-25).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Kuribayashi's teaching of designing LSI involves many EDA (electronic design automation) tools in respective stages. These tools are

essential for automatically designing ASICs such as memories, in particular, SRAMs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further improve to meet requirements for large-scale memories and a short turn around time

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc in view of Kuribayashi and further in view Gupte.

As to claim 7, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated". Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

As to claim 8, Duboc discloses the claimed limitation subject matter in claim 6, except the claimed limitation "wherein the script file relating to each of said selected selectors is automatically generated according to a pre-prepared template". Duboc

teaches a template may also generate one or more script files (col. 10, lines 58-60). Gupte teaches automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs (col.13, lines 25-35).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Gupte's teaching of automatically generates design specific synthesis scripts for use with a synthesis tool after receiving user's inputs to Duboc's system in order to eliminate the need for a user to manually generate a test of the ASIC or eliminate complex tasks when debugging the scripts and further help the entire design to complete accurately and efficiently.

10. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duboc et al (or hereinafter "Duboc") (US 6425116) in view of Kuribayashi and further in view of Hekmatpour (US 2002/0156929).

As to claim 10, Duboc and Kuribayashi disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared template is a pre-prepared external file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Kuribayashi's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of

functional components that includes simulator and synthesis and timing analysis component.

As to claim 11, Duboc and Kuribayashi disclose the claimed limitation subject matter in claim 8, except the claimed limitation "wherein the pre-prepared external template file is an XML file". Hekmatpour teaches XML file, which is represented as an external file (fig. 4, page 3, col. Left, line 41).

It would have been obvious to a person of an ordinary skill in the art at the time the invention was made to apply Hekmatpour's teaching of XML file to Duboc's system and Kuribayashi's system in order to provide a system for enabling collaborative design and verification of a system on a chip (Soc) and further to generate a plurality of functional components that includes simulator and synthesis and timing analysis component.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cam Y T Truong whose telephone number is (571) 272-4042. The examiner can normally be reached on Monday to Firday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cam-Y Truong
Patent Examiner
Art Unit 2162
7/18/2005

SHAHID ALAM
PRIMARY EXAMINER